CERTIFICATION OF TRANSLATION

I, Jeonghee Lee, an employee of Y.P.LEE, MOCK & PARTNERS of The Cheonghwa Bldg., 1571-18 Seocho-dong, Seocho-gu, Seoul, Republic of Korea, hereby declare under penalty of perjury that I understand the Korean language and the English language; that I am fully capable of translating from Korean to English and vice versa; and that, to the best of my knowledge and belief, the statements in the English language in the attached translation of the priority document (Korean Patent Application No. 02-65610), consisting of 37 pages, have the same meanings as the statements in the Korean language in the original document, a copy of which I have examined.

Signed this 28 day of January, 2005

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ABSTRACT

[Abstract of the Disclosure]

A ferroelectric memory device using a via etch-stop layer and a method for manufacturing the same are provided. The ferroelectric memory device includes a plurality of ferroelectric capacitors disposed two-dimensionally on a lower interlayer insulating layer in the row direction and the column direction. The tops of the ferroelectric capacitors are exposed through an interlayer insulating layer covering between the ferroelectric capacitors. A patterned via etch-stop layer is formed only on the interlayer insulating layer. A plurality of plate lines each is electrically connected to the ferroelectric capacitors on at least two neighboring rows and contact the patterned via etch-stop layer between the ferroelectric capacitors. Accordingly, high integration is achieved since a via hole is not required in each cell for connection of plate lines. Further, the lower interlayer insulating layer is protected by the patterned via etch-stop layer, preventing the capacitor characteristics from being degraded.

[Representative Drawing]

FIG. 9.

SPECIFICATION

[Title of the Invention]

FERROELECTRIC MEMORY DEVICE USING VIA ETCH-STOP LAYER AND METHOD FOR MANUFACTURING THE SAME

[Brief Description of the Drawings]

FIGS. 1 through 9 are cross-sectional views of a ferroelectric memory device and a method for manufacturing the same according to an embodiment of the present invention.

FIGS. 10 through 15 are cross-sectional views of a ferroelectric memory device and a method for manufacturing the same according to another embodiment of the present invention.

<Explanation of Reference Numerals Designating the Major Elements of the Drawings>

20: First lower interlayer insulating layer

35: Second lower interlayer insulating layer

60: Ferroelectric capacitor

70: Interlayer insulating layer

80a, 180a: Patterned via etch-stop layer

90: Encapsulated barrier layer

95, 195: First upper interlayer insulating layer 105a: Strapping line

110, 210: Second upper interlayer insulating layer

115, 215: Slit-shaped common via hole 120, 220: Plate line

[Detailed Description of the Invention]

[Object of the Invention]

[Technical Field of the Invention and Related Art prior to the Invention]

The present invention relates to a semiconductor device, and more particularly, to a ferroelectric memory device including a ferroelectric capacitor and a method for manufacturing the same.

Recently, ferroelectric memory devices using a ferroelectric layer have been recognized as the memory devices for the next generation. The ferroelectric memory device works by controlling the direction of polarization according to the direction of an applied electric field, and a digital 0 or 1 is stored according to the

direction of remnant polarization when the electric field is removed. This kind of ferroelectric memory device is characterized by high endurance, high speed of tens of nanoseconds, low driving voltage of less than 5V and low power dissipation. However, the ferroelectric memory device must be more integrated to be used as a memory product, besides the characteristics.

To achieve high integration of the ferroelectric memory device, it is necessary not only to embody the cell structure of 1T/1C (1 transistor/1 ferroelectric capacitor), miniaturize the ferroelectric capacitor, and develop multiple wiring processes, but also to guarantee hot temperature retention, and powerful writing and reading abilities compared to DRAM and SRAM.

Especially, miniaturization of the ferroelectric capacitor becomes the most important and complicated technology as high integration technology progresses. This is because changes of the ferroelectricity have not yet been fully verified according to ferroelectric capacitor regions obviously reduced by the high integration, and subsequent processes for the reduced capacitors have become more difficult. In addition, via holes in each cell need to be connected to plate lines according to the characteristics of the ferroelectric memory device. The conventional method for manufacturing via holes in each cell is not available in a capacitor region with a design rule less than 0.25μm.

Therefore, there is a need for new technology for forming via holes to be connected to plate lines in a reduced capacitor. This technology should not damage the capacitor. In general, a damage might occur due to etching chemicals (gas or solution), and this can degrade the capacitor by degrading the remnant polarization or its distribution. Especially, if the distribution of remnant polarization in each capacitor is irregular, it reduces the sensing margin in a ferroelectric memory device. This is because the process method of a ferroelectric memory device is based on comparing the remnant polarization of both a reference cell capacitor and a memory cell capacitor and recognizing the difference between them.

[Technical Goal of the Invention]

It is an object of the present invention to provide a more integrated ferroelectric memory device, by improving the connection between plate lines and a ferroelectric capacitor.

It is another object of the present invention to provide a method for manufacturing a ferroelectric memory device including methods for forming via holes

in manufacturing a highly integrated ferroelectric memory device, without any problems relating to degrading the characteristic of a capacitor.

[Structure and Operation of the Invention]

To accomplish the object of the present invention, in an embodiment, a ferroelectric memory device comprises a plurality of ferroelectric capacitors disposed two-dimensionally on a lower interlayer insulating layer formed on a semiconductor substrate in the row direction and the column direction. The tops of the ferroelectric capacitors are exposed through an interlayer insulating layer covering between the ferroelectric capacitors. A patterned via etch-stop layer is formed only on the interlayer insulating layer. An upper interlayer insulating layer is formed on the patterned via etch-stop layer. A plurality of plate lines each is electrically connected to the ferroelectric capacitors on at least two neighboring rows and contact the via etch-stop layer between the ferroelectric capacitors.

The patterned via etch-stop layer is made of a material having a different etch selectivity from the interlayer insulating layer and the upper interlayer insulating layer. For example, if the interlayer insulating layer and the upper interlayer insulating layer are made of an oxide layer, the patterned via etch stop layer is made of a titanium oxide layer (TiO_2), an aluminium oxide layer (Al_2O_3), a silicon nitride layer (Si_3N_4), or a silicon oxynitride layer (SiON).

An encapsulated barrier layer is clad on the patterned via etch-stop layer and deters permeation of hydrogen. The encapsulated barrier layer is made of an aluminum oxide layer, a titanium oxide layer, a zirconium oxide layer (ZrO_2), a tantalum oxide layer (Ta_2O_5), a silicon nitride layer, or a cesium oxide layer (CeO_2).

On the while, the ferroelectric capacitors include a lower electrode, a ferroelectric layer pattern, and an upper electrode layer sequentially, and the plate lines directly contact the upper electrodes on at least two neighboring rows. At this time, the plate lines are common plate lines which directly contact the upper electrodes on at least two neighboring rows through a slit-shaped common via hole passing through the upper interlayer insulating layer.

In another embodiment of the present invention, a ferroelectric memory device comprises a plurality of ferroelectric capacitors disposed two-dimensionally on a lower interlayer insulating layer formed on a semiconductor substrate in the row direction and the column direction. An interlayer insulating layer is formed to fill a region between the ferroelectric capacitors to the same height as the ferroelectric

capacitors, leaving a top surface of the ferroelectric capacitors exposed. A patterned via etch-stop layer is formed on the interlayer insulating layer, leaving the top surface of the interlayer insulating layer exposed between at least two adjacent ferroelectric capacitors. An upper interlayer insulating layer is formed on the patterned via etch-stop layer. A plurality of plate lines are formed such that each plate line is electrically connected to the ferroelectric capacitors on at least two neighboring rows.

The ferroelectric memory device may further comprise an encapsulating barrier layer formed between the ferroelectric capacitors and the interlayer insulating layer or within the upper interlayer insulating layer to prevent permeation of hydrogen.

To accomplish another object of the present invention, in an embodiment, a method for manufacturing a ferroelectric memory device comprises forming a lower interlayer insulating layer on a semiconductor substrate. A plurality of ferroelectric capacitors are formed two-dimensionally on the lower interlayer insulating layer, in the row direction and the column direction. An interlayer insulating layer covering the ferroelectric capacitors and a via etch-stop layer are sequentially formed. The via etch-stop layer and the interlayer insulating layer are patterned to form cell via holes which expose the tops of the ferroelectric capacitors. A first upper interlayer insulating layer is formed to completely fill the cell via holes. Strapping lines are formed on a top of the first upper interlayer insulating layer. A second upper interlayer insulating layer is formed to entirely cover the strapping lines. A plurality of plate lines are formed to each electrically access the ferroelectric capacitors on at least two neighboring rows and contact the patterned via etch-stop layer between the ferroelectric capacitors by etching the second upper interlayer insulating layer and the first upper interlayer insulating layer using the patterned via etch-stop layer as an etch finishing point and depositing a conductive layer.

The via etch-stop layer is made of a material having a different etch selectivity from the interlayer insulating layer, the first upper interlayer insulating layer, and the second upper interlayer insulating layer. The interlayer insulating layer, the first upper interlayer insulating layer, and the second upper interlayer insulating layer are made of an oxide layer, and the via etch-stop layer is made of a titanium oxide layer, an aluminium oxide layer, a silicon nitride layer, or a silicon oxynitride layer.

The forming of the ferroelectric capacitors comprises sequentially forming a lower electrode layer, a ferroelectric layer and an upper electrode layer on the lower interlayer insulating layer; and patterning the upper electrode layer, the ferroelectric layer and the lower electrode layer continuously to form a plurality of ferroelectric layers in which the lower electrode, the ferroelectric layer pattern and the upper electrode are layered sequentially.

The plate lines are common plate lines that directly contact the ferroelectric capacitors on at least the two neighboring rows through a slit-shaped common via hole penetrating the first and second upper interlayer insulating layers.

In another embodiment of the present invention, a method for manufacturing a ferroelectric memory device comprises forming a lower interlayer insulating layer on a semiconductor substrate. A plurality of ferroelectric capacitors are formed two-dimensionally on the lower interlayer insulating layer, in the row direction and the column direction. An interlayer insulating layer is formed to cover the ferroelectric capacitors and is then planarized until a top surface of the ferroelectric capacitors is exposed. A via etch-stop layer is formed on an entire surface of the semiconductor substrate including the planarized interlayer insulating layer. A first upper interlayer insulating layer is forming on the via etch-stop layer. Strapping lines are formed over the first upper interlayer insulating layer. A second upper interlayer insulating layer is formed to cover the strapping lines. A slit-shaped common via hole is formed by selectively etching the second and first upper interlayer insulating layers between the at least two adjacent ferroelectric capacitors using the via etch-stop layer as an etch end point. The top surface of the ferroelectric capacitors is exposed by etching the via etch-stop layer within the slit-shaped common via hole without etching the second and first upper interlayer insulating layers and the interlayer insulating layer. A plate line is formed by depositing a conductive layer within the slit-shaped common via hole to commonly contact at least two adjacent ferroelectric capacitors and to contact the interlayer insulating layer between the at least two ferroelectric capacitors.

According to the present invention, since plate lines and capacitors are connected through a slit-shaped common via hole, elements restricting integration are removed in forming via holes for the connection of plate lines in each cell. In addition, a via etch-stop layer is used as an etch finish point, thus preventing damage to the lower interlayer insulating layer. This overcomes the conventional

problem in that a capacitor characteristic is degraded by permeation of etching chemicals into a dielectric layer.

The present invention now will be described more fully with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete and, will fully convey the concept of the present invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. It will also be understood that when a layer is referred to as being "on" another layer or a substrate, it can be directly on the other layer or the substrate, or interlayer layers may also be present. In drawings, the same reference numerals represent the same element.

<First Embodiment>

FIG. 9 shows a sectional view of a ferroelectric memory device according to an embodiment of the present invention. According to the present invention, cell transistors are disposed two-dimensionally on the semiconductor substrate in the row direction and the column direction. FIG. 9 shows a sectional view cut along a column perpendicular to the row direction of an extension of the gate of each cell transistor.

Referring to FIG. 9, a plurality of cell transistors are formed on the semiconductor substrate 10 of which an isolation process is completed. A cell transistor includes a gate 15, a source region 17 and a drain region 18 at both sides of the gate 15. A contact pad 25 is formed on top of a source region 17 and a drain region 18. A bit line 30 is electrically connected to the drain region 18 of the cell transistors passing through the first lower interlayer insulating layer 20 by the contact pad 25. A second lower interlayer insulating layer 35 is also formed and contact plugs 40 are formed on top of the drain region 18 passing through the second lower interlayer insulating layer 35 and the first lower interlayer insulating layer 20. The contact plugs 40 are electrically connected to the source regions 17 of the cell transistors by the contact pads 25. The contact pads 25 are formed when the aspect ratio of each contact hole for forming the bit line 30 and the contact plug 40, is large, and thus, are sometimes omitted.

On top of the contact pads 25 are formed the ferroelectric capacitors 60. The cell transistors and contact plugs 40 are two-dimensionally disposed, and consequently, the ferroelectric capacitors 60 are also two-dimensionally disposed.

Each ferroelectric capacitor 60 includes a lower electrode 45, a ferroelectric layer pattern 50 and an upper electrode 55, layered sequentially. The lower electrode 45 is located on top of the contact plug 40 and is electrically connected to the source region 17 through the contact plug 40. Further, the lower electrode 45 consists of multiple layers including an adhesive layer, a lower diffusion barrier layer, a lower metallic oxide layer and a lower metallic layer. The total thickness of the lower electrode can range from 1000 to 3000 Å. The lower diffusion barrier layer is formed to prevent oxygen from diffusing. For example, the lower diffusion barrier layer is made of a metal, i.e., TiN, Ti, TiAlN, TiSix, TiSi, TiSiN, TaSiN, TaAlN, Ir, Ru, W, or WSi, with a high melting point, its silicide, or its nitride. The ferroelectric layer pattern 50 is made of a $Pb(Zr, Ti)O_3$ layer, a $SrBi_2Ta_2O_9$ layer or $SrBi(Ta, Nb)_2O_9$. In addition, the ferroelectric layer pattern 50 may be made of a $SrTiO_3$ layer, a $BaTiO_3$ layer, a $(Ba,Sr)TiO_3$ layer, a $(Pb,La)(Zr,Ti)O_3$ layer, or a $Bi_4Ti_3O_{12}$ layer. The upper electrode 55 can be a dual layer of an upper metallic oxide layer and an upper diffusion barrier layer. The total thickness of the upper electrode can also range from 1000 to 3000 Å. The upper electrode 55 and the lower electrode 45 are made of a metal such as Pt, Ir, Ru, Rh, Os, Pd, etc. Accordingly, their metallic oxides such as IrO_2, RhO_2 or RuO_2 also can be used for the upper electrode 55 and the lower electrode 45.

The upper electrode 55 of the ferroelectric capacitor 60 is exposed by the interlayer insulating layer 70 which covers the regions between the ferroelectric capacitors 60. A patterned via etch-stop layer 80a is made only on the interlayer insulating layer 70. On top of the patterned via etch-stop layer 80a is clad an encapsulated barrier layer 90. The encapsulated barrier layer 90 can be a metallic oxide layer such as an aluminum oxide layer, a titanium oxide layer, a zirconium oxide layer, a tantalum oxide layer, a silicon nitride layer, or a cerium oxide layer.

This kind of encapsulated barrier layer 90 can prevent hydrogen atoms generated during manufacture or included in carrier gas from permeating the ferroelectric layer pattern 50. If hydrogen atoms permeate the ferroelectric layer pattern 50 they reduce the reliability of the ferroelectric layer pattern 50 by reacting to oxygen atoms inside the ferroelectric layer pattern 50 to produce oxygen

vacancies, which degrade the polarization characteristics of the ferroelectric capacitor. Consequently, this leads to the malfunction of the ferroelectric memory device.

In addition, if hydrogen atoms spread in the interface between the ferroelectric layer pattern 50, the upper electrode 55 and the lower electrode 45, the energy barrier between them is lowered degrading the leakage current characteristics of the ferroelectric capacitor. As a result, the encapsulated barrier layer 90 improves the characteristics and reliability of the ferroelectric capacitor 60.

An upper interlayer insulating layer is formed on the patterned via etch-stop layer 80a. The upper interlayer insulating layer includes a first upper interlayer insulating layer 95 and a second upper interlayer insulating layer 110. The patterned via etch-stop layer 80a is preferably formed of a material having a different etch selectivity from the interlayer insulating layer 70 and the upper interlayer insulating layer (95, 110). For example, if the interlayer insulating layer 70 and the upper interlayer insulating layer (95, 110) are made of an oxide layer, the patterned via etch-stop layer 80a is preferably made of a titanium oxide layer, an aluminum oxide layer, a silicon nitride layer, or a silicon oxynitride layer. A plurality of strapping lines 105a are formed between the first upper interlayer insulating layer 95 and the second upper interlayer insulating layer 110, thereby forming a first wiring.

A plurality of plate lines 120 for a second wiring are formed directly in contact with the ferroelectric capacitors 60 disposed on at least two neighboring rows through a slit-shaped common via hole 115 passing through the second upper interlayer insulating layer 95, the first upper interlayer insulating layer 110, and the encapsulated barrier layer 90. These plate lines 120 contact the patterned via etch-stop layer 80a between the ferroelectric capacitors 60.

As described in detail, each plate line is connected with at least two capacitors through a slit-shaped common via hole, removing elements which restrict integration in forming via holes for connection of plate lines in each cell. Therefore, such a ferroelectric memory device can be more highly integrated by improving the connecting structure with plate lines in a reduced capacitor according to reductions of the design rule.

Hereinafter, a method for manufacturing a ferroelectric memory device according to an embodiment of the present invention is described. FIGS. 1 through

8 are cross-sectional views showing a method for manufacturing a ferroelectric memory device according to the embodiment of the present invention in FIG. 9.

As shown in FIG. 1, a plurality of cell transistors are formed two-dimensionally on the semiconductor substrate 10 after an isolation process, in the row direction and in the column direction. After forming a plurality of gates, a source region 17 and a drain region 18 are formed on the semiconductor substrate 10 at both sides of each gate 15 by implanting impurities. A conductive layer of the gate 15 can be made of doped polycrystalline silicon, tungsten (W), tungsten silicide (WSi), titanium silicide (TiSix), tantalum silicide (TaSix) or combinations thereof. A cell transistor includes the gate 15, the source region 17 and a drain region 18 at both sides of the gate 15. Next, the contact pad 25 is formed on the source region 17 and the drain region 18. The contact pad 25 can be formed of doped polycrystalline silicon and can be self-aligned.

After forming the first lower interlayer insulating layer 20 on the semiconductor substrate 10, on which the contact pad 25 is formed, a bit line 30 is formed to be electrically connected to the drain region 18 of the cell transistor by passing through the first lower interlayer insulating layer 20 by the contact pad 25. The first lower interlayer insulating layer 20 can be made of, for example, BPSG (Boro Phospho Silicate Glass), and the bit line 30 can be made of, for example, tungsten.

After forming the second lower interlayer insulating layer 35 on the semiconductor substrate 10, on which the bit line 30 is formed, a plurality of contact plugs 40 are formed to be electrically connected to the source region 17 of the cell transistor by passing through the second lower interlayer insulating layer 35 and the first lower interlayer insulating layer 20 by the contact pad 25. The second lower interlayer insulating layer 35 can also be made of BPSG, and the contact plugs 40 can be made of, for example, doped polycrystalline silicon.

In addition, a lower electrode layer, a ferroelectric layer and an upper electrode layer are formed sequentially on top of the second lower interlayer insulating layer 35 including the contact plugs 40. The lower electrode layer can be formed of multiple layers including an adhesive layer, a lower diffusion barrier layer, a lower metallic oxide layer and a lower metallic layer and its total thickness can range between 1000 and 3000Å. The adhesive layer is formed to make a lower electrode in ohmic contact with the contact plugs 40. The adhesive layer can be formed by depositing a titanium layer to a thickness of 100-500Å using a sputtering

process and changing the titanium layer into a titanium oxide layer by performing heat treatment using oxygen in a furnace. The adhesive layer may sometimes be omitted. It should be noted that the lower diffusion barrier layer is formed to prevent oxygen from diffusing. For example, the lower diffusion barrier layer can be formed by depositing a metal, i.e., TiN, Ti, TiAlN, TiSix, TiSi, TiSiN, TaSiN, TaAlN, Ir, Ru, W, or WSi, with a high melting point, its silicide, or its nitride using a physical vapor deposition (PVD) method such as sputtering, a chemical vapor deposition (CVD) method, or a sol-gel method. When the adhesive layer is omitted, the lower diffusion barrier layer is in ohmic contact with the contact plugs 40. It is most preferable that the lower diffusion barrier is made of Ir with a low oxygen permeability in order to satisfactorily prevent oxygen from diffusing. The upper electrode layer can be a dual layer including an upper metallic oxide layer, and an upper diffusion barrier layer. The total thickness thereof can range from about 1000 and 3000Å. The upper diffusion barrier layer can be made of the same material as the lower diffusion barrier layer. The upper electrode and the lower electrode are made of a metal such as Pt, Ir, Ru, Rh, Os, Pd and the oxides thereof. For example, the lower electrode layer can be composed of Ir with a thickness of 1500Å, IrO_2 with a thickness of 500Å, and Pt with a thickness of 1500Å. The upper electrode layer can be composed of Ir with a thickness of 300Å and IrO_2 with a thickness of 1200Å. These components of the lower and upper electrode layers can be formed using PVD. The ferroelectric layer is made of a $Pb(Zr, Ti)O_3$ layer, a $SrBi_2Ta_2O_9$ layer or $SrBi(Ta, Nb)_2O_9$ using spin coating, or LSMCD (Liquid Source Mist Chemical Vapor Deposition), chemical vapor deposition (CVD) or physical vapor deposition (PVD). Preferably, when the ferroelectric layer is made of a $Pb(Zr,Ti)O_3$ layer, the $Pb(Zr,Ti)O_3$ layer is formed by performing crystallization heat treatment after sol-gel process. In addition, the ferroelectric layer can be made of a $SrTiO_3$ layer, a $BaTiO_3$ layer, a $(Ba,Sr)TiO_3$ layer, a $(Pb,La)(Zr,Ti)O_3$ layer, or a $Bi_4Ti_3O_{12}$ layer.

A lower electrode layer, a ferroelectric layer and an upper electrode layer are patterned using a mask, to form a plurality of ferroelectric capacitors, in which a lower electrode layer 45, a ferroelectric layer pattern 50 and an upper electrode 55 are sequentially stacked. The ferroelectric capacitors 60 are formed on the contact plugs 40. Since the cell transistors are disposed in a two-dimensional array, therefore, the contact plugs 40 and the ferroelectric capacitors 60 are also disposed in a two-dimensional array.

It is not possible to etch using the existing three masks, because an overlay margin is considerably reduced in a highly integrated ferroelectric memory device. Instead, a capacitor node separation is performed by general photo etching using a single hard mask layer made of a titanium nitride layer and a photoresist.

Next, as shown in FIG. 2, an interlayer insulating layer 70 covering the ferroelectric capacitor 60 is formed. A via etch-stop layer 80 is then formed on the interlayer insulating layer 70. The interlayer insulating layer 70 can be made of, for example, USG(Undoped Silicate Glass), PSG(Phosphorus Silicate Glass), PE-TEOS(Plasma Enhanced Tetra Ethyl Ortho Silicate Glass), or combinations of various insulation films. The via etch-stop layer 80 is made of a material having a different etch selectivity from the interlayer insulating layer 70 and comprises, for example, e a titanium oxide layer, an aluminum oxide layer, a silicon nitride layer, or a silicon oxynitride layer.

Referring to FIG. 3, the via etch-stop layer 80 and the interlayer insulating layer 70 are patterned in each cell, thereby forming cell via holes 85 exposing the upper electrodes 55. Reference numeral 80a denotes the patterned via etch-stop layer.

Next, as shown in FIG. 4, an encapsulating barrier layer 90 is formed on the patterned via etch-stop layer 80a to prevent hydrogen from permeating. The encapsulating barrier layer 90 can be, for example, an aluminum oxide layer, a titanium oxide layer, a zirconium oxide layer, a tantalum oxide layer, a silicon nitride layer, or a cerium oxide layer. Further, the encapsulating barrier layer 90 can prevent hydrogen atoms generated during semiconductor fabrication or included in a carrier gas from permeating through the ferroelectric layer pattern 50. As described above, hydrogen atoms should be excluded from the semiconductor devices as much as possible. This is because hydrogen diffuses into the ferroelectric capacitor layer pattern 50 through the upper electrode 55, thereby deoxidizing the oxidized substances in the ferroelectric layer pattern 50. As a result, the ferroelectric characteristics are degraded and adhesion to the upper electrode 55 of the ferroelectric layer pattern 50 is decreased due to changes in the chemical properties of the interface. The upper electrode 55 is elevated by by-products such as oxygen and water, which are produced in an oxidation-reduction reaction. The upper electrode 55 and the ferroelectric layer pattern 50 therefore easily liftoff at the interface. Accordingly, hydrogen atoms are excluded by the encapsulating barrier

layer 90. The encapsulating barrier layer 90 can be formed by PVD using ion metal plasma (IMP) or collimate method in order to improve a step coverage or CVD. Alternatively, the encapsulating barrier layer 90 can be formed by PE-CVD, LP (low pressure)-CVD, AP (atmospheric pressure)-CVD, or atomic layer deposition (ALD). In particular, since ALD can be performed at low temperature, the encapsulating barrier layer 90 physically and chemically stabilized can be formed. Furthermore, a single atomic layer is repeatedly formed, so it is possible to exactly control the thickness of the encapsulating barrier layer 90. Accordingly, the encapsulating barrier layer 90 can be formed to have a 100% step coverage regardless of the complexity of topology of an underlying surface.

Referring to FIG. 5, a first upper interlayer insulating layer 95 is formed over the patterned via etch-stop layer 80a. The first upper interlayer insulating layer 95 fills the cell via hole 85. It is preferable that the first upper interlayer insulating layer 95 be made of another material having a different etch selectivity from the patterned via etch-stop layer 80a. If a titanium oxide layer, an aluminum oxide layer, a silicon nitride layer, or a silicon oxynitride layer is used as the patterned via etch-stop layer 80a, an oxide layer can be used as the first upper interlayer insulating layer 95. For example, the first upper interlayer insulating layer 95 can be made of USG, PSG, or PE-TEOS. A conductive layer 105 is then formed on the first upper interlayer insulating layer 95. As the conductive layer 105, a layer of metal such as aluminum can be used.

Referring to FIG. 6, strapping lines 105a are formed on the first upper interlayer insulating layer 95 by patterning the conductive layer 105. The strapping lines 105a are formed at opposite sides of two adjacent cell via holes 85 such that the two adjacent cell via holes 85 are disposed between the strapping lines 105a.

As shown in FIG. 7, a second upper interlayer insulating layer 110 is formed overlying the strapping lines 105a. If the strapping lines 105a and their subsequently formed plate lines are made of metal, the second upper interlayer insulating layer 110 may be an intermetal insulating layer. Preferably, the second upper interlayer insulating layer 110 is made of a material having a different etch selectivity from the patterned via etch-stop layer 80a. Accordingly, like the first upper interlayer insulating layer 95, the second upper interlayer insulating layer 110 can be formed of an oxide layer such as USG, PSG, or PE-TEOS.

Referring to FIG. 8, the second upper interlayer insulating layer 110 and the first upper interlayer insulating layer 95 are etched to form a common via hole 115, using the patterned via etch-stop layer 80a as an etch end point. The common via hole 115 exposes the upper electrodes 55 of the adjacent capacitors 60. The common via hole 115 is preferably slit-shaped. The slit-shaped common via hole 115 overlaps with the cell via holes 85 therebelow. However, a person skilled in the art will appreciate that other shapes can be also used depending on applications. The slit-shaped common via hole 115 preferably exposes the upper electrodes 55 of at least two adjacent capacitors 60, but more upper electrodes may be exposed.

An encapsulating barrier layer 90, exposed in the above etching process, is also etched. The patterned via etch-stop layer 80a protects the interlayer insulating layer 70 between the ferroelectric capacitors 60 from being etched, because the via etch-stop layer 80 is formed of a material having a different etch selectivity from the interlayer insulating layer 70, the first upper interlayer insulating layer 95, and the second upper interlayer insulating layer 110. Accordingly, etching chemicals do not permeate the ferroelectric layer pattern 50, and the ferroelectric capacitors 60 are not degraded. In the regions without the patterned via etch-stop layer 80a, the second upper interlayer insulating layer 110 and the first upper interlayer insulating layer 95 are etched. Then, the upper electrodes 55 of the ferroelectric capacitors 60 are exposed.

Turning to FIG. 9, plate lines 120 are formed by depositing a conductive layer, for example, a metal such as aluminum, on the resulting structure to form a ferroelectric memory device. The plate lines 120 are electrically connected to the at least two adjacent ferroelectric capacitors 60 via the common via hole 115, and are in contact with the patterned via etch-stop layer 80a between the ferroelectric capacitors 60. Instead aluminum, the plate lines 120 can be made of any material having conductivity. When the plate lines 120 are made of aluminum, a CVD or sputtering method can be used. The sputtering method does not require a high-temperature reflow process because it is performed in the wide slit-shaped common via hole 115, so the degradation of characteristics of the ferroelectric capacitors 60 can be avoided.

As described above, when a slit-shaped via hole is formed using the via etch-stop layer as an etch end point according to an embodiment of the present invention, the lower interlayer insulating layer is not damaged. Accordingly, etching

chemicals do not expose the ferroelectric layer pattern or lower electrode, so they do not damage the capacitors. Consequently, degradation of remnant polarization or its distribution can be avoided.

<Second Embodiment>

FIGS. 10 through 15 are cross-sectional views of a ferroelectric memory device and a method for manufacturing the same according to a second embodiment of the present invention. According to this embodiment, cell transistors are disposed on the semiconductor substrate in a two-dimensional array of perpendicular rows and columns. The elements having the same functions as those shown in FIGS. 1 through 9 are denoted by the same reference numerals, and a detailed description thereof will be omitted. The second embodiment is different from the first embodiment in that an interlayer insulation layer is planarized before a via etch-stop layer is formed.

Referring to FIG. 15, which shows the structure of a ferroelectric memory device, the upper electrode 55 of each ferroelectric capacitor 60 is exposed through an interlayer insulating layer 170 that fills the regions between the ferroelectric capacitors 60. Here, the height of the interlayer insulating layer 170 is the same as that of each ferroelectric capacitor 60. A patterned via etch-stop layer 180a is formed on the interlayer insulating layer 170, exposing the interlayer insulating layer 170 between the ferroelectric capacitors 60 in at least two neighboring rows.

The patterned via etch-stop layer 180a is covered with an upper interlayer insulating layer (195, 210). The patterned via etch-stop layer 180a is formed of a material having a different etch selectivity from the interlayer insulating layer 170 and the upper interlayer insulating layer. For example, if the interlayer insulating layer 170 and the upper interlayer insulating layer (195, 210) are made of an oxide layer, the patterned via etch-stop layer 180a is preferably made of a titanium oxide layer, an aluminum oxide layer, a silicon nitride layer, or a silicon oxynitride layer.

The upper interlayer insulating layer includes a first upper interlayer insulating layer 195 and a second upper interlayer insulating layer 210. The plurality of strapping lines 105a are formed between the first upper interlayer insulating layer 195 and the second upper interlayer insulating layer 210. A plurality of plate lines 220 are formed in direct contact with the ferroelectric capacitors 60 in at least two neighboring rows through a slit-shaped common via hole 215 that passes through the second upper interlayer insulating layer 210 and the first upper interlayer

insulating layer 195. The plate lines 220 contact the interlayer insulating layer 170 between the ferroelectric capacitors 60.

Although not shown, an encapsulated barrier layer (denoted by reference numeral 90 in FIG. 9) can also be formed between the ferroelectric capacitors 60 and the interlayer insulating layer 170 or within the first and second upper interlayer insulating layers 195 and 210 to prevent permeation of hydrogen.

In a ferroelectric memory device having such a structure, instead of forming a via hole for connection of a plate line in each cell, a slit-shaped common vial hole is formed to connect a plate line to at least two capacitors, so the ferroelectric memory device can be more readily highly integrated.

Hereinafter, a method for manufacturing a ferroelectric memory device having the structure shown in FIG. 15 will be described with reference to FIGS. 10 through 14.

As shown in FIG. 10, the process described with reference to FIG. 1 in the first embodiment are performed until the lower electrode layer, the ferroelectric layer and the upper electrode layer are patterned using a mask, to form a plurality of ferroelectric capacitors 60, in which the lower electrode layer 45, the ferroelectric layer pattern 50 and the upper electrode 55 are sequentially stacked. Next, the ferroelectric capacitors 60 are covered with the interlayer insulating layer 170. The interlayer insulating layer 170 can be made of a material such as USG, PSG, or PE-TEOS.

Next, as shown in FIG. 11, the interlayer insulating layer 170 is planarized. The planarization can be performed using etch-back or chemical-mechanical polishing (CMP) until the upper electrodes 55 of the ferroelectric capacitors 60 are exposed, thereby removing the interlayer insulating layer 170 from top of the ferroelectric capacitors 60 and leaving the interlayer insulating layer 170 only in the region between the ferroelectric capacitors 60. Conditions for stages in the planarization are adjusted so that the planarization is stopped at a level not damaging the upper electrode 55. Next, a via stop-etch layer 180 is formed on the entire surface of the semiconductor substrate 10 including the planarized interlayer insulating layer 170. The via etch-stop layer 180 is made of a material having a different etch selectivity from the interlayer insulating layer 170 and comprises, for example, a titanium oxide layer, an aluminum oxide layer, a silicon nitride layer, or a silicon oxynitride layer. When the via etch-stop layer 180 is made of a conductive

material, it is necessary to separately form a via etch-stop layer for each cell using photolithography.

Next, as shown in FIG. 12, the first upper interlayer insulating layer 195 is formed on the via etch-stop layer 180. The first upper interlayer insulating layer 195 is preferably made of a material, for example, USG, PSG, or PE-TEOS, having a different etch selectivity from the via etch-stop layer 180. A conductive layer such as an aluminum layer is formed on the first upper interlayer insulating layer 195 and is then patterned to form the strapping lines 105a.

Subsequently, as shown in FIG. 13, the second upper interlayer insulating layer 195 is formed on the resulting structure having the strapping lines 105. The second upper interlayer insulating layer 195 can also be made of USG, PSG, or PE-TEOS.

Next, as shown in FIG. 14, the slit-shaped common via hole 215 exposing the upper electrodes 55 of adjacent capacitors 60. In the sectional view, it is seen like the slit-shaped common via hole 215 exposes the upper electrodes 55 of two capacitors 60. However, in a plan view, the slit-shaped common via hole 215 exposes more upper electrodes. Preferably, the slit-shaped common via hole 215 exposes the upper electrodes of ferroelectric capacitors on at least two rows. Here, the second upper interlayer insulating layer 210 and the first upper interlayer insulating layer 195 are selectively etched using the via etch-stop layer 180 as an etch end point. The slit-shaped common via hole 215 preferably exposes the upper electrodes 55 of at least two adjacent capacitors 60, but more upper electrodes may be exposed. The via etch-stop layer 180 protects the interlayer insulating layer 170 between the ferroelectric capacitors 60 from being etched during the formation of the slit-shaped common via hole 215, because the via etch-stop layer 180 is formed using a material having a different etch selectivity from the interlayer insulating layer 170, the first upper interlayer insulating layer 195, and the second upper interlayer insulating layer 210. Accordingly, etching chemicals do not permeate the ferroelectric layer pattern 50, and the ferroelectric capacitors 60 are not degraded.

Next, FIG. 15 shows the result of exposing the top surfaces of the ferroelectric capacitors 60 by removing the via etch-stop layer 180 within the slit-shaped common via hole 215 without etching the second upper interlayer insulating layer 210, the first upper interlayer insulating layer 195, and the interlayer insulating layer 170 and then forming the plate lines 220. When the top surfaces of the ferroelectric capacitors 60

are exposed, the via etch-stop layer 180 is patterned. Reference numeral 180a denotes the patterned via etch-stop layer. The via etch-stop layer 180 can be removed using, for example, an RF sputtering method using argon. By adjusting the conditions, only the via etch-stop layer 180 can be removed without damaging the interlayer insulating layer 170. Here, the plate lines 220 are electrically connected to the at least two adjacent ferroelectric capacitors 60 via the common via hole 215 and are in contact with the interlayer insulating layer 170 between the ferroelectric capacitors 60.

If the via etch-stop layer 180 does not exist, when the slit-shaped common via hole 215 is formed, the interlayer insulating layer 170 is excessively recessed, exposing the ferroelectric layer patterns 50. Accordingly, when the plate lines 220 are formed thereafter, the ferroelectric layer patterns 50 are in direct contact with the plate lines 220, thereby degrading ferroelectric characteristics. When the interlayer insulating layer 170 is excessively over etched, the plate lines 220 contact the lower electrodes 45, causing short circuit, so a defective ferroelectric memory device is produced. However, according to the second embodiment of the present invention using the via etch-stop layer, the ferroelectric layer patterns 50 and the lower electrodes 45 are prevented from being exposed during an etching process using etching chemicals, so a robust ferroelectric memory device can be manufactured. In addition, the uniformity of remnant polarization is maintained in each ferroelectric capacitor 60, which overcomes the problem of reduction of sensing margin in a ferroelectric memory device.

As described above, when a slit-shaped common via hole is formed using a via etch-stop layer or a via etch-stop layer pattern as an etch end point according to the second embodiment of the present invention, the interlayer insulating layer is not damaged. This overcomes the conventional problem where etching chemicals permeate the capacitor dielectric layer and degrade the capacitor characteristics.

It should be noted that the present invention is not limited to the embodiments described above, and it is apparent that variations and modifications can be made by those skilled in the art. For example, each of the plate lines can be connected to at least three neighboring capacitors.

[Effect of the Invention]

As described above, plate lines and capacitors are connected through a slit-shaped common via hole according to an embodiment of the present invention,

improving integration in forming via holes for connection of plate lines in each cell. According to an embodiment of the present invention, a plate line is in direct contact with the upper electrodes of the at least two adjacent ferroelectric capacitors in a cell array. Accordingly, integration of the ferroelectric memory device is considerably increased. In addition, the reliability of the ferroelectric memory device is greatly improved.

Further, since a via etch-stop layer or a via etch-stop layer pattern is used as an etch end point, the lower interlayer insulating layer is not damaged. This overcomes the problem of the prior art, where etching chemicals permeate the capacitor dielectric layer and degrade the capacitor characteristics. Thus, a very reliable capacitor with highly improved characteristics can be manufactured according to embodiments of the present invention.

What is claimed is:

1. A ferroelectric memory device comprising:

a lower interlayer insulating layer formed on a semiconductor substrate;

a plurality of ferroelectric capacitors disposed on the lower interlayer insulating layer two-dimensionally in a row direction and a column direction;

an interlayer insulating layer formed over the ferroelectric capacitors, leaving a top surface of the ferroelectric capacitors exposed;

a patterned via etch-stop layer formed only on the interlayer insulating layer;

an upper interlayer insulating layer formed on the patterned via etch-stop layer; and

a plurality of plate lines each electrically connected to ferroelectric capacitors on at least two adjacent rows and contacting the patterned via etch-stop layer disposed between the ferroelectric capacitors.

2. The ferroelectric memory device of claim 1, wherein the patterned via etch-stop layer is made of a material having a different etch selectivity from the interlayer insulating layer and the upper interlayer insulating layer.

3. The ferroelectric memory device of claim 2, wherein the interlayer insulating layer and the upper interlayer insulating layer comprise an oxide layer, and the patterned via etch-stop layer is made of a material layer selected from the group consisting of a titanium oxide layer, a silicon nitride layer, a silicon oxynitride layer, and an aluminum oxide layer.

4. The ferroelectric memory device of claim 1, further comprising an encapsulating barrier layer that covers the patterned via etch-stop layer to prevent permeation of hydrogen.

5. The ferroelectric memory device of claim 4, wherein the encapsulating barrier layer comprises an oxide layer selected from the group consisting of an aluminum oxide layer, a titanium oxide layer, a zirconium oxide layer, a tantalum oxide layer, a silicon nitride layer, and a cerium oxide layer.

6. The ferroelectric memory device of claim 1, wherein each ferroelectric capacitor includes a lower electrode, a ferroelectric layer pattern and an upper electrode layer, and wherein each of the plate lines directly contacts the upper electrodes of the ferroelectric capacitors on at least two adjacent rows.

7. The ferroelectric memory device of claim 6, wherein the plate line is a common plate line that directly contacts the upper electrodes of the ferroelectric capacitors on at least two adjacent rows through a slit-shaped common via hole penetrating the upper interlayer insulating layer.

8. The ferroelectric memory device of claim 7, wherein the interlayer insulating layer and the patterned via etch-stop layer define cell via holes that expose a top surface of the ferroelectric capacitors, and the cell via holes overlap with the slit-shaped common via hole.

9. The ferroelectric memory device of claim 1, wherein the lower interlayer insulating layer comprises:

a plurality of cell transistors disposed on the semiconductor substrate two-dimensionally in the row direction and the column direction;

a plurality of bit lines electrically connected to drain regions of the cell transistors; and

a plurality of contact plugs electrically connected to source regions of the cell transistors,

wherein the ferroelectric capacitors electrically contact the source regions through the contact plugs.

10. The ferroelectric memory device of claim 7, wherein the upper interlayer insulating layer comprises:

a first upper interlayer insulating layer and a second upper interlayer insulating layer, which are sequentially stacked, and

strapping lines disposed at both sides of the slit-shaped common via hole between the first upper interlayer insulating layer and the second upper interlayer insulating layer.

11. A method for manufacturing a ferroelectric memory device, the method comprising:

forming a lower interlayer insulating layer on a semiconductor substrate;

forming a plurality of ferroelectric capacitors on the lower interlayer insulating layer two-dimensionally in a row direction and a column direction;

sequentially forming an interlayer insulating layer and a via etch-stop layer, overlying the ferroelectric capacitors;

patterning the via etch-stop layer and the interlayer insulating layer to form cell via holes that expose a top surface of the ferroelectric capacitors;

forming a first upper interlayer insulating layer to fill the cell via holes;

forming strapping lines over the first upper interlayer insulating layer;

forming a second upper interlayer insulating layer covering the strapping lines; and

forming a plurality of plate lines by etching the second upper interlayer insulating layer and the first upper interlayer insulating layer using the patterned via etch-stop layer as an etch end point and depositing a conductive layer, the plate lines being electrically connected to ferroelectric capacitors on at least two adjacent rows and contacting the patterned via etch-stop layer between the ferroelectric capacitors.

12. The method of claim 11, wherein the via etch-stop layer is made of a material having a different etch selectivity from the interlayer insulating layer, the first upper interlayer insulating layer, and the second upper interlayer insulating layer.

13. The method of claim 12, wherein the interlayer insulating layer, the first and second upper interlayer insulating layers are made of an oxide layer, and the via etch-stop layer is made of a layer selected from the group consisting of a titanium oxide layer, a silicon nitride layer, a silicon oxynitride layer, and an aluminum oxide layer.

14. The method of claim 11, further comprising forming an encapsulating barrier layer on the patterned via etch-stop layer to deter permeation of hydrogen after patterning the via etch-stop layer and the interlayer insulating layer.

15. The method of claim 14, wherein the encapsulating barrier layer is made of an oxide layer selected from the group consisting of an aluminum oxide layer, a titanium oxide layer, a zirconium oxide layer, a tantalum oxide layer, a silicon nitride layer, and a cerium oxide layer.

16. The method of claim 11, wherein forming the ferroelectric capacitors comprises:

sequentially forming a lower electrode layer, a ferroelectric layer and an upper electrode layer on the lower interlayer insulating layer; and

sequentially patterning the upper electrode layer, the ferroelectric layer and the lower electrode layer to form the plurality of ferroelectric capacitors, in which a lower electrode, a ferroelectric layer pattern and an upper electrode are sequentially stacked.

17. The method of claim 11, wherein the plate lines are common plate lines that directly contact ferroelectric capacitors on at least two adjacent rows through a slit-shaped common via hole penetrating the first upper interlayer insulating layer and the second upper interlayer insulating layer.

18. The method of claim 14, wherein the plate lines are common plate lines that directly contact ferroelectric capacitors on at least two adjacent rows through a slit-shaped common via hole penetrating the first upper interlayer insulating layer, the second upper interlayer insulating layer and the encapsulating barrier layer.

19. The method of claim 16, wherein the ferroelectric layer is made of a layer selected from the group consisting of a $Pb(Zr, Ti)O_3$ layer, a $SrBi_2Ta_2O_9$ layer and $SrBi(Ta, Nb)_2O_9$.

20. The method of claim 11, before forming the lower interlayer insulating layer, the method further comprises:

forming a plurality of cell transistors on the substrate of the semiconductor two-dimensionally in the row direction and the column direction;

forming a first lower interlayer insulating layer on the semiconductor substrate having the plurality of cell transistors;

forming a plurality of bit lines electrically connected to the drain regions of the cell transistors through the first lower interlayer insulating layer;

forming a second lower interlayer insulating layer on the entire surface of the semiconductor substrate having the bit lines; and

forming a plurality of contact plugs which electrically connect the ferroelectric capacitor and the source regions of the cell transistors through the second lower interlayer insulating layer and the first interlayer insulating layer.

21. A ferroelectric memory device comprising:

a lower interlayer insulating layer formed on a semiconductor substrate;

a plurality of ferroelectric capacitors disposed on the lower interlayer insulating layer two-dimensionally in a row direction and a column direction;

an interlayer insulating layer filling a region between the ferroelectric capacitors to the same height as the ferroelectric capacitors;

a patterned via etch-stop layer formed on the interlayer insulating layer, leaving the interlayer insulating layer exposed between ferroelectric capacitors on at least two adjacent rows;

an upper interlayer insulating layer formed on the patterned via etch-stop layer; and

a plurality of plate lines each electrically connected to the ferroelectric capacitors on at least two adjacent rows.

22. The ferroelectric memory device of claim 21, wherein the patterned via etch-stop layer is made of a material having a different etch selectivity from the interlayer insulating layer and the upper interlayer insulating layer.

23. The ferroelectric memory device of claim 22, wherein the interlayer insulating layer and the upper interlayer insulating layer comprise an oxide layer, and the patterned via etch-stop layer is made of a material layer selected from the group consisting of a titanium oxide layer, a silicon nitride layer, a silicon oxynitride layer, and an aluminum oxide layer.

24. The ferroelectric memory device of claim 21, further comprising an encapsulating barrier layer formed between the ferroelectric capacitors and the

interlayer insulating layer or within the upper interlayer insulating layer to prevent permeation of hydrogen.

25. The ferroelectric memory device of claim 24, wherein the encapsulating barrier layer comprises an oxide layer selected from the group consisting of an aluminum oxide layer, a titanium oxide layer, a zirconium oxide layer, a tantalum oxide layer, a silicon nitride layer, and a cerium oxide layer.

26. The ferroelectric memory device of claim 21, wherein the ferroelectric capacitors each include a lower electrode, a ferroelectric layer pattern and an upper electrode layer, and wherein the plate lines directly contact the upper electrodes of the ferroelectric capacitors on at least two adjacent rows.

27. The ferroelectric memory device of claim 21, wherein the plate lines are common plate lines directly contacting the ferroelectric capacitors on at least two adjacent rows through a slit-shaped common via hole passing through the upper interlayer insulating layer.

28. A method for manufacturing a ferroelectric memory device, the method comprising:

forming a lower interlayer insulating layer on a semiconductor substrate;

forming a plurality of ferroelectric capacitors on the lower interlayer insulating layer two-dimensionally in a row direction and a column direction;

forming an interlayer insulating layer covering the ferroelectric capacitors and planarizing the interlayer insulating layer until a top surface of the ferroelectric capacitors is exposed;

forming a via etch-stop layer on an entire surface of the semiconductor substrate including the planarized interlayer insulating layer;

forming a first upper interlayer insulating layer on the entire surface of the semiconductor substrate including the via etch-stop layer;

forming strapping lines over the first upper interlayer insulating layer;

forming a second upper interlayer insulating layer covering the strapping lines;

forming a slit-shaped common via hole by selectively etching the second and first upper interlayer insulating layers between ferroelectric capacitors on at least two adjacent rows using the via etch-stop layer as an etch end point;

exposing the top surface of the ferroelectric capacitors by etching the via etch-stop layer within the slit-shaped common via hole without etching the second and first upper interlayer insulating layers and the interlayer insulating layer; and

forming a plurality of plate lines by depositing a conductive layer within the slit-shaped common via hole to be electrically connected to the ferroelectric capacitors on at least two adjacent rows and to contact the interlayer insulating layer between the ferroelectric capacitors.

29. The method of claim 28, wherein the via etch-stop layer is made of a material having a different etch selectivity from the interlayer insulating layer, the first upper interlayer insulating layer, and the second upper interlayer insulating layer.

30. The method of claim 29, wherein the interlayer insulating layer, the first and second upper interlayer insulating layers are made of an oxide layer, and the via etch-stop layer is made of a layer selected from the group consisting of a titanium oxide layer, a silicon nitride layer, a silicon oxynitride layer, and an aluminum oxide layer.

31. The method of claim 28, wherein the interlayer insulating layer is planarized using an etch-back process or chemical-mechanical polishing process.

32. The method of claim 28, further comprising forming an encapsulating barrier layer between the ferroelectric capacitors or within the first or second upper interlayer insulating layer to prevent permeation of hydrogen.

33. The method of claim 32, wherein the encapsulating barrier layer comprises an oxide layer selected from the group consisting of an aluminum oxide layer, a titanium oxide layer, a zirconium oxide layer, a tantalum oxide layer, a silicon nitride layer, and a cerium oxide layer.

FIG. 1

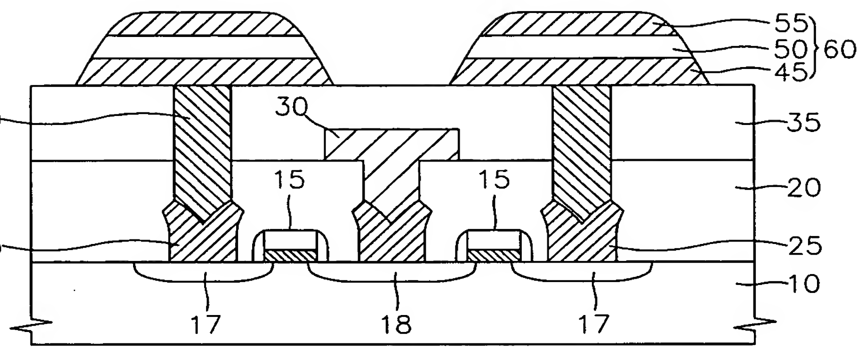
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FIG. 2

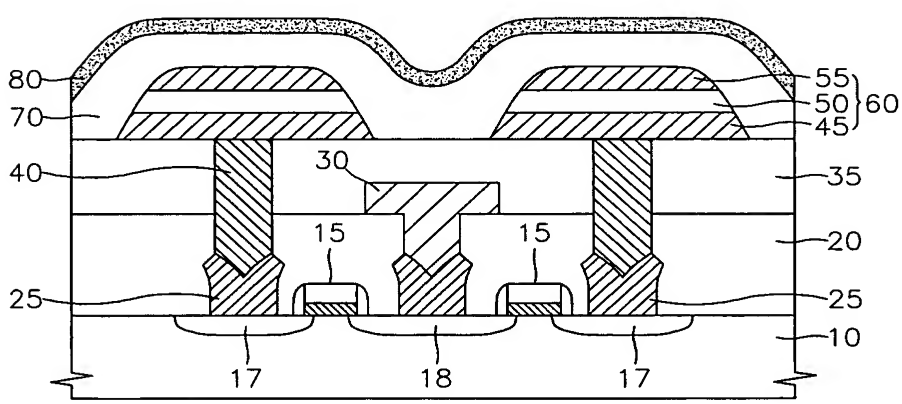
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FIG. 3

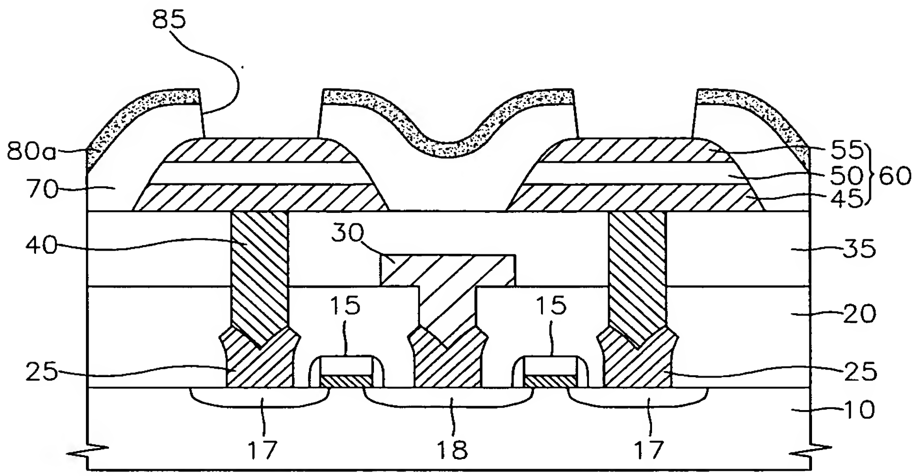
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FIG. 4

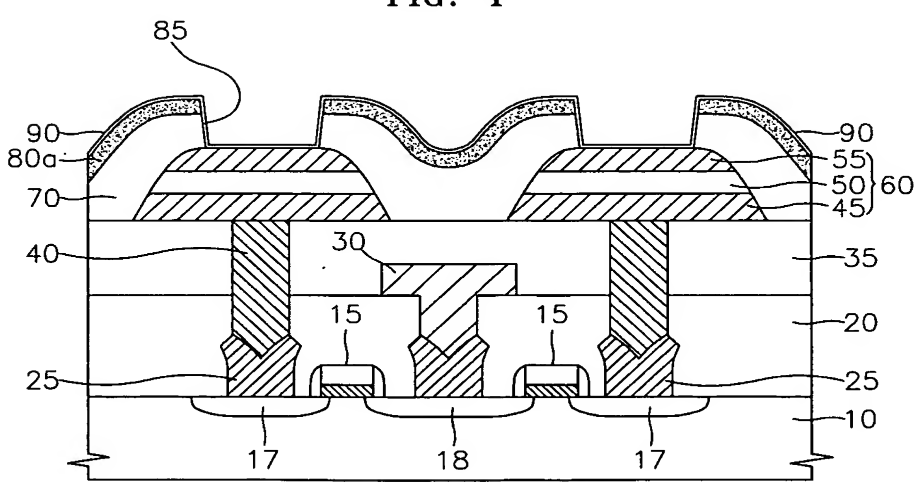
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FIG. 5

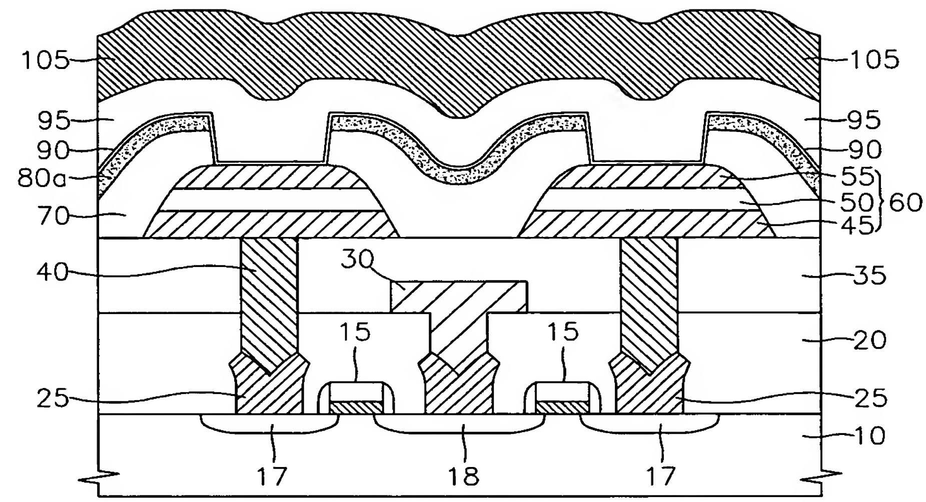
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FIG. 6

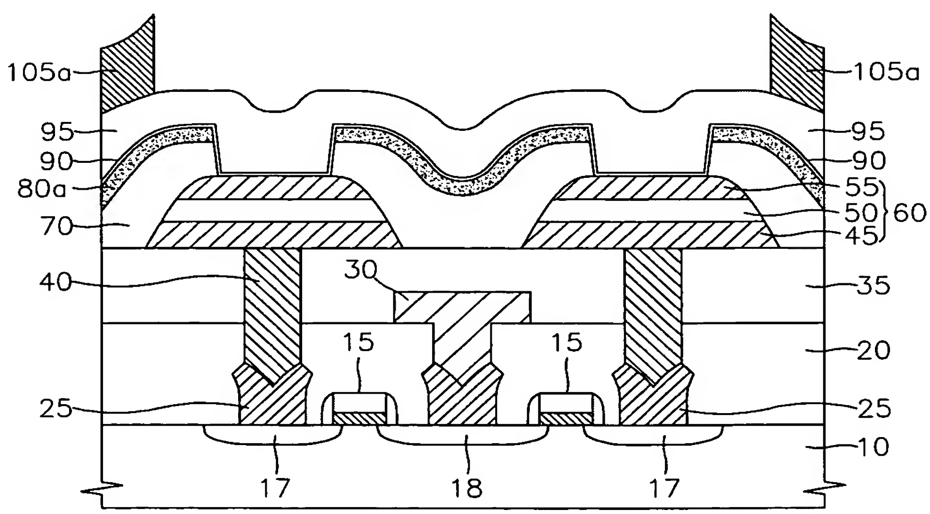
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FIG. 7

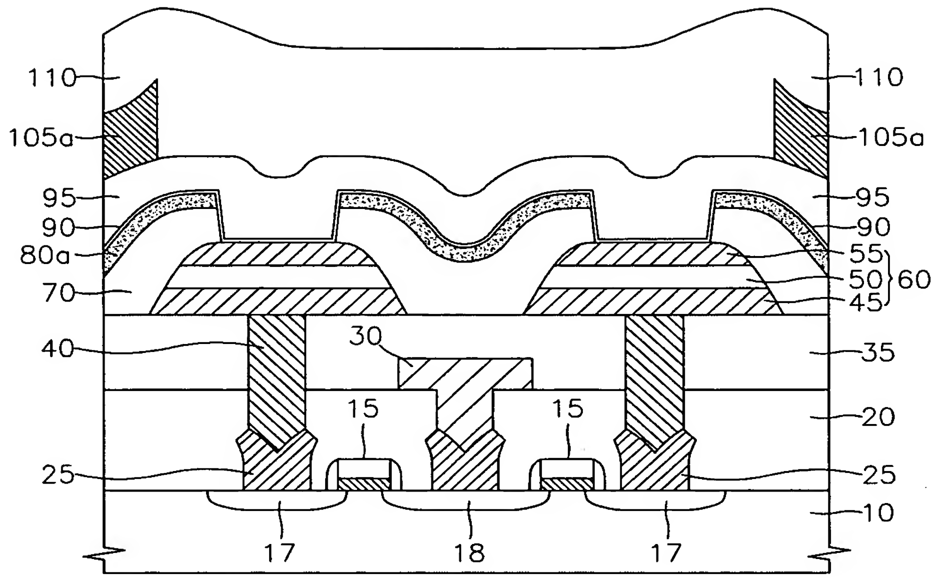
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FIG. 8

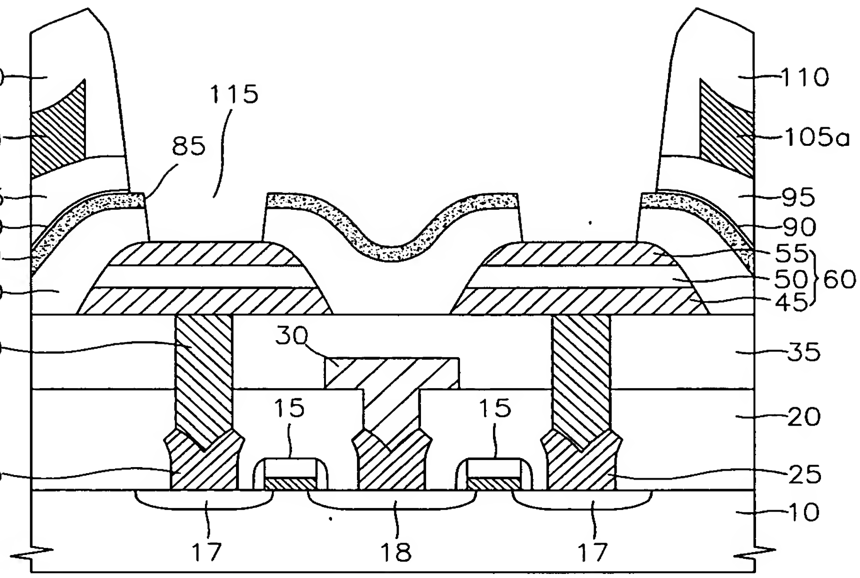
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FIG. 9

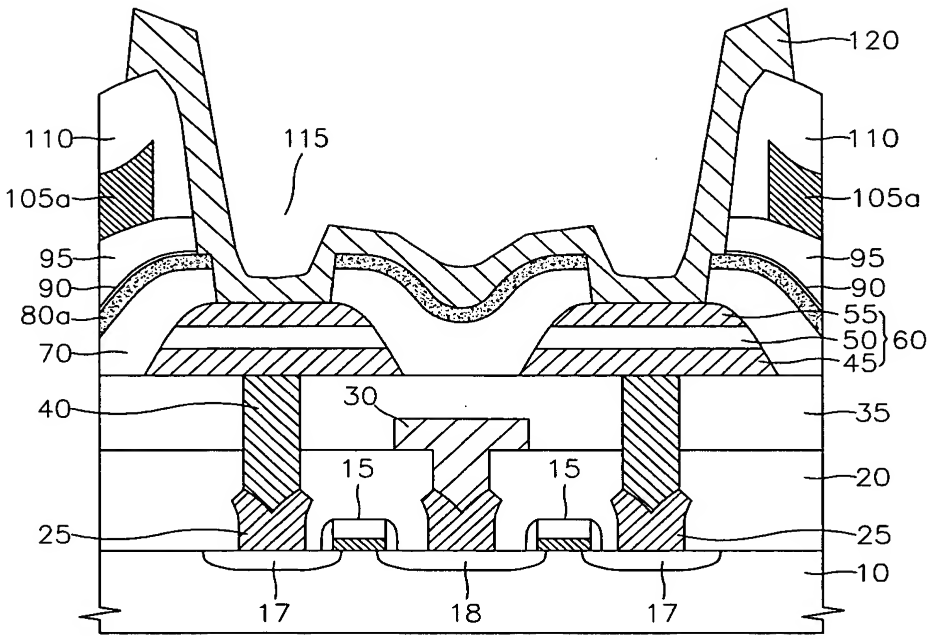

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FIG. 10

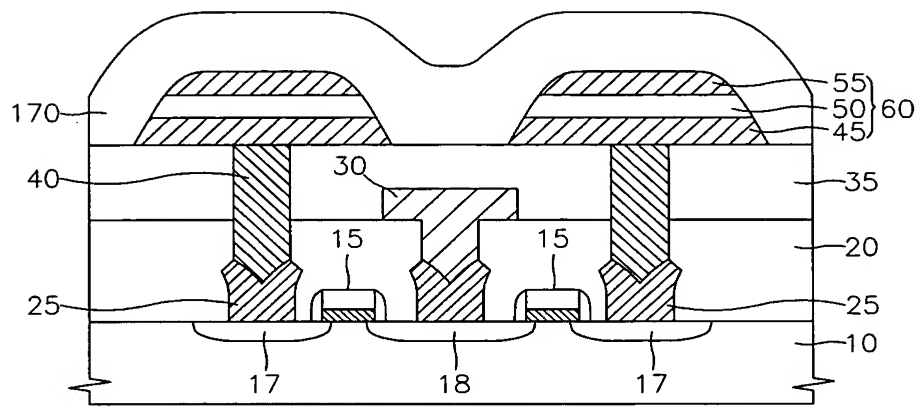

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FIG. 11

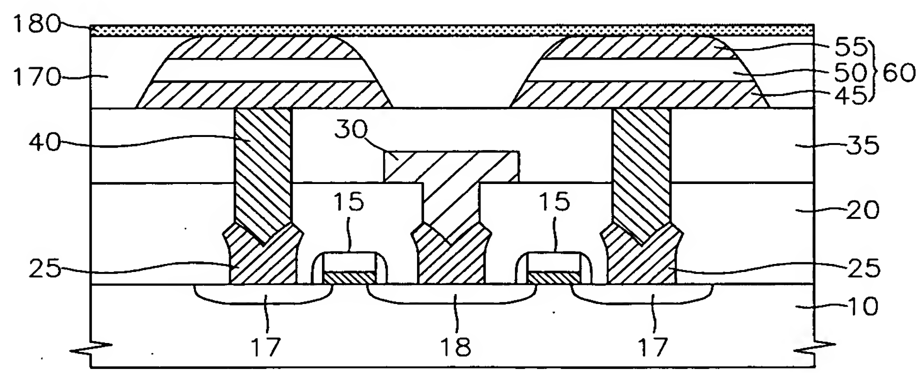

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FIG. 12

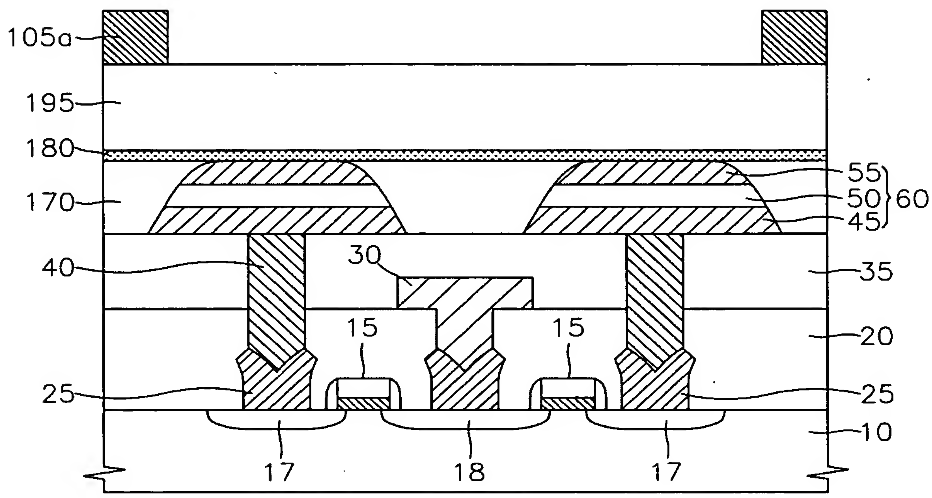

FIG. 13

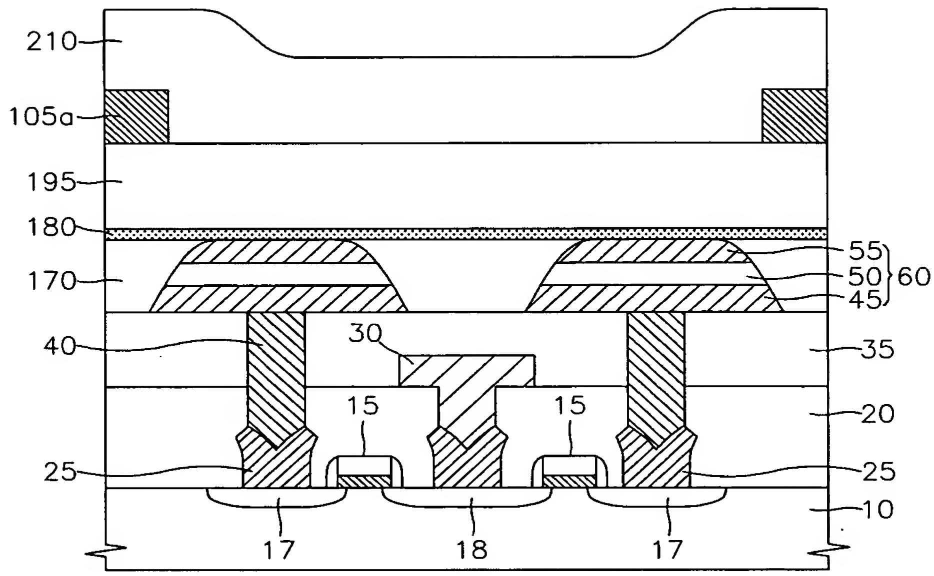

FIG. 14

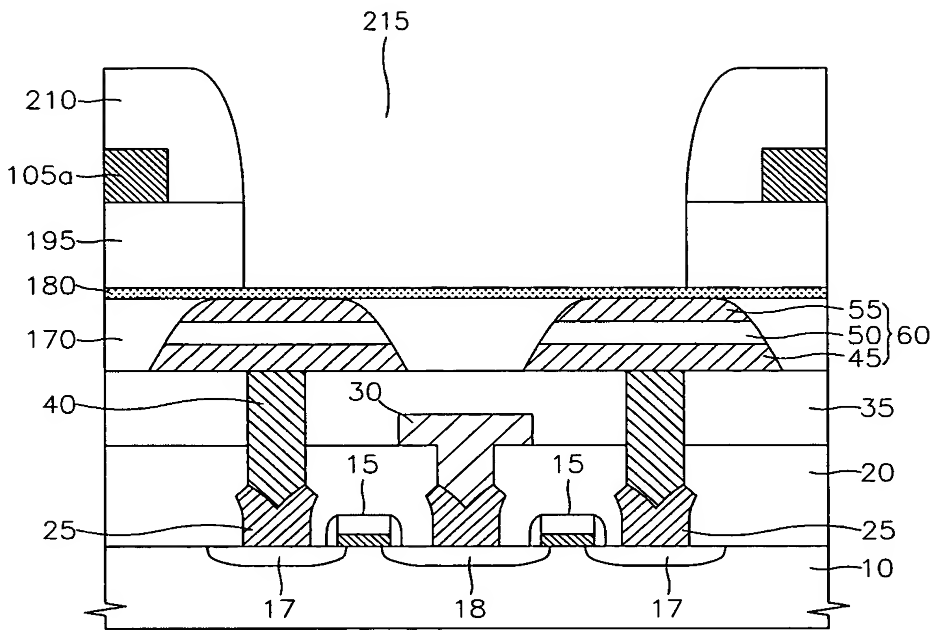

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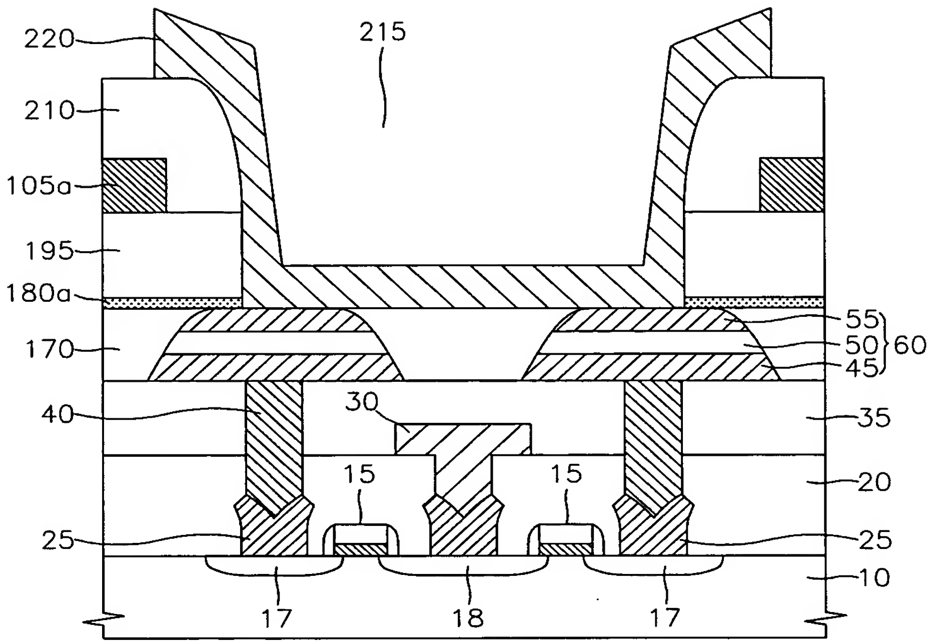
FIG. 15



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